## IN THE SPECIFICATION

Please replace the paragraph beginning at page 13, line 9, with the following rewritten paragraph:

--As stated above, circuit performance of the dynamic SOI logic circuits of the instant invention can be improved using low threshold voltage techniques such as electrically connecting the transistor gate to the floating body of the SOI transistor. The gate-to-body connection can be applied to the PMOS transistors and NMOS transistors in a PDN. A gate to floating body connection 310 is shown in Figure 7 for a PMOS transistor in the PDN 267. The gate-to-body connection utilizes the body effect of the MOSFET transistor to lower the threshold voltage thus improving the transistor performance. The SOI dynamic logic circuits described in the instant invention can also be applied to bulk CMOS circuits. Thus the embodiments of the invention illustrated in Figures 4 – 7 can be applied to bulk substrates that do not have a buried dielectric layer. In the bulk CMOS embodiment of the instant invention, the source/drain diffusions of the PMOS transistor will not abut the source/drain diffusions of the NMOS transistor under current bulk CMOS transistor isolation schemes. The advantages gain by using the disclosed static logic design over existing bulk CMOS static logic designs will be in the speed and performance of the logic circuits. --

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